

SUITE BRIDGES ESL TO SOC DESIGN

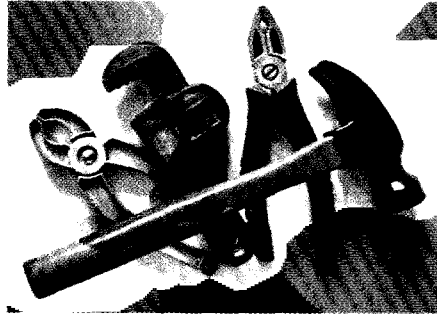
ESL affords a high level of abstraction, higher than RTL (register transfer level) but steers clear of converting the high-level representation, or models, into implementation equivalents.

ESL languages, such as hardware-centric MatLab and software-centric C and C++, represent the behaviours of a system before hardware and software partitioning. The ESL languages can also be used to represent the system's hardware and/or its software portions.

ESL capture tools capture the high level models, either as language editors or graphical environments, while ESL exploration, analysis and visualisation tools are self-explanatory in their roles in system design. With the hardware/software design that still exists, this can be evaluating various hardware/software partitions or analysing the effectiveness of different architectures for portions of a design.

Tool types

ESL synthesis, translation and compilation tools are used to track the models, for example converting into RTL which is transferred into conventional synthesis and



processor. Vast (www.vastsystems.com) is an example of the latter, all encompassing, approach.

Increasing speeds

One offering of behavioural synthesis reports an increase in speed and an easier connection to link a system design into the ever-growing legion of physical, SoC designs. Celoxica (www.celoxica.com) announced the DK4 to support the synthesis of these larger and more complex designs.

Memory holds the key to SoC design, according to the company. This fourth-generation DK Design Suite for C synthesis links ESL design and synthesis to SoC design by placing C synthesis in the embedded

ESL (electronic system level) design provides the designer with concurrent models for analysis, exploration and verification in hardware and software parts of a system. But how can it improve SoC design, asks CAROLINE HAYES

Synopsys's Design Compiler (www.synopsys.com). The tool supports automatic scripting for SoC testbench generation as well as RTL input for the SoC flow. By optimising the connection from C language to RTL to Synopsys's Design Compiler tool, it bridges the gap between ESL and and physical SoC design.

Silicon from software

The company's C-synthesis tools automatically generate optimised FPGA netlists from high-level descriptions. With improved technology mapping, the company claims that it helps designers leverage the embedded ALU (arithmetic logic unit) features and DSP blocks in high-density FPGAs, and cites Altera's Stratix II and Xilinx's Virtex 4 as well as the latter's high-density Spartan3E and low power Spartan 3L devices. All popular FPGA devices can be targeted by algorithm designs using a new GUI (graphic user interface) for an intuitive software to silicon design flow.

The DK Design Suite is available on Windows OS and the company has now also made it available to Linux OS users. **EPP**

Suite enhancements are claimed to enable an easier integration into the software to silicon process

simulation environments or converting into a gate-level, or look-up table netlist, as they migrate into an implementation level equivalent for production.

While some companies focus on different levels of this progression, others offer full system simulation tools to examine architecture choices and optimisation for hardware/software partitioning, before adopting these representations as reference models for hardware and as virtual platforms to develop embedded software. Examples of the former are Tensilica (www.tensilica.com) which takes C/C++ source code to generate a custom processor and Stretch (www.stretchinc.com), which uses it to configure the programmable portion of a

standard SoC design flow. It reports an increase in speed of 30 to 50 per cent over previous versions.

The increase in memory capacity increases design capacity and speeds synthesis execution. FPGA implementations can be produced directly from large software models. As the tool is not limited to small, single block, single clock modules, it can synthesise complete systems, encompassing complex algorithms, system interfaces and multiple clock domains.

Enhancements

Suite enhancements are claimed to enable an easier integration into the software to silicon process. New VHDL and Verilog output optimisations interface with

