

Joint wafers go mainstream

CHIP FOUNDRIES ARE moving from making multiproject wafers (MPW) a sideline for smaller customers to get prototypes, to being a key part of their portfolios. This is in order to convince potential users of advanced processes that they can produce silicon affordably. Alongside the MPW runs, the foundries are beginning to offer access to smaller lot sizes because many designs do not have large enough die sizes to demand full wafer lots that satisfy quarterly or even annual demand.

As a result, MPW runs will be among the first commercial offerings that foundries such as Singapore-based **Chartered Semiconductor** will offer.

Kevin Meyer, vice-president of worldwide marketing for Chartered Semiconductor, said: "We are planning to do MPW as a key part of our strategy. Even large customers value multiproject wafers for proving their libraries or design elements ahead of committing to an actual product design. We also have

customers at the leading edge of new applications that are not always as funded as some of the large customers."

Chartered plans to run its first MPW for the 65nm process in the fourth quarter of this year and start production by the second quarter of 2006. The Singapore company developed its 90nm process jointly with IBM and extended the partnership to include Infineon and Samsung for a 65nm offering.

Dr Walt Lange, field executive for system solutions at **IBM**, said: "Our

*Foundries such as **Chartered and IBM** plan to use shared masks to make 65nm processes accessible*

first 65nm MPW is scheduled to be released imminently and we do have test sites from customers on that for the 65nm low-power process." Lange added that mask costs are now so prohibitive that most customers develop their prototypes on MPW, not just startups and smaller players.

Meyer said: "The mask cost is a challenge for the industry and we do subsidise a lot of that for the early development, and work with our customers to ensure that, economically, it is not prohibitive for them getting to volume, which is both of our end goals. One of the things we are doing to obviate some of the costs of developing advanced 90nm and 65nm technology is going to smaller lot sizes so, as customers bring their products out, they don't have to fill a complete wafer boat with wafers. We can do some small lot processing to support them early on when they don't need [full lots], to lower some of the cost on the front end."

Dual proof

IBM and Chartered Semiconductor are using the multiproject wafer (MPW) approach to prove their semiconductor IP on each other's manufacturing lines, partly to help ensure the processes remain in exact alignment.

"One of the key elements of the relationship with IBM is this 'process exact' approach where we match the process being brought up in the IBM fab so our customers have the ability to design on process and have it run on IBM," said Kevin Meyer, vice-president of worldwide marketing for Chartered.

The two companies have also developed a common set of design rule checks so they can have a common GDSII format, and have done joint library negotiations with Virage and Artisan to do single implementations of their libraries on top of the joint process.

"Customers are increasing their investments in 90nm and 65nm designs. They're looking for single design, multi-sourcing strategies," Meyer added.