

VARIED APPROACHES TO EMBEDDED SOCS

Maximising processor performance and reducing the cost and complexity of SoCs can be achieved by multi-core and superscalar architectures. Alternatively, multi-threading can be used in embedded applications, writes CAROLINE HAYES

In embedded processor design today, there is a dichotomy between CPU frequencies and memory speeds, which has impacted on processor and SoC designs. While the average CPU frequency increases by a factor of two every two years, DRAM speeds, for example, only increase by a factor of two every six years. As applications incur higher frequencies, traditional processor methodologies can be less efficient, as the memory latencies increase. While the processor is waiting for the memory element to respond, the processor is likely to stall. The higher frequencies and the latency gap also increase power consumption.

Superscalar architectures can suffer from an increase in area size as well as low efficiency, which can reduce the effect of any performance gains. Multi-core processing can deliver performance gains but at a penalty in that it can increase the die size and raise the power consumption levels.

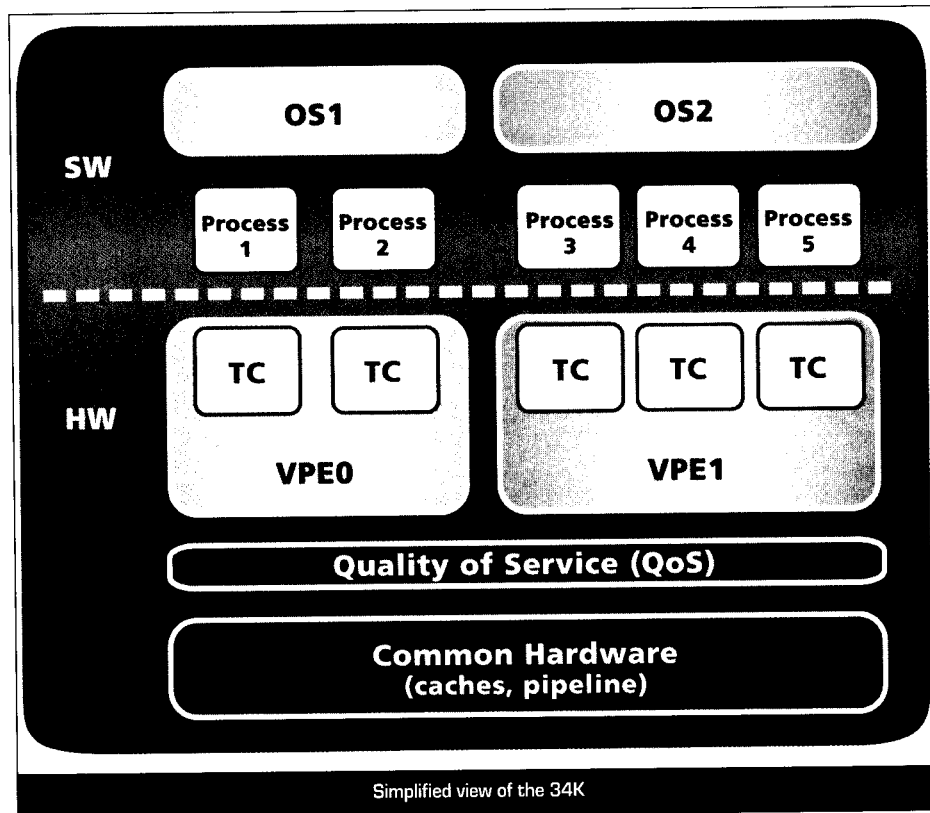
Multi-threading is a popular concept, as multiple threads, fed through a processor's pipeline can be executed without cycle wait times which delay a single-threaded microprocessor. As a result, multi-threaded processors can save throughput times, maximise performance but the trade-off for this can be a significant increase in die size.

Multi-threading cores

In a bid to balance system performance with reducing system costs in SoCs, MIPS Technologies (www.mips.com) has released the 34K family of multi-threading cores. They

Internal benchmarks rated the 34Kc core, running two threads was 60 per cent faster than a single-threaded processor

join the company's 24K and 24KE cores for single-threaded applications. With multi-thread and DSP extensions, the cores can deliver up to twice the level of performance



over previous generations. The 90nm technology cores has a worst case frequency rating of 500MHz on a 2.1mm² core size with a power consumption of 0.56mW/MHz@1V (core only). The 34K cores are designed specifically for multi-threaded workloads and use the company's MT Application Specific Extension (ASE). They

The 32bit synthesizable core has a nine-stage, single-issue pipeline and includes an optional inter-thread communications unit and an optional floating point unit. The 64bit memory sub-system is divided into integrated, four-way set-associative write-back caches and nine out-of-order, non-blocking loads. There is an optional data scratchpad with a DMA port. To enhance clock gating, the power management is fine grained to account for the increase in performance speed.

Spreading the load

The multi-threaded workload applications can

are based on the 24KE micro-architecture that includes MIPS DSP ASE, which integrates the DSP function in addition to the RISC instruction set on the same core.

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be single applications with specific threads, for example VoIP channels in domestic applications. The core could also be used to merge several single-threaded functions onto a single core, as in a host processor, running Linux and a DSP running an RTPOS in a set-top box application. The cores can also be used in network routers and digital TV or DVD recorders, which require a level of workload concurrency. Early adoption licensees include PMC-Sierra, in its next-generation SoCs and Mobileye, in the Netherlands, which has used the multi-

Processing bandwidth within the core can be allocated to real-time tasks, increasing the responsiveness levels in embedded applications. This can monitor the progress of the threads and take corrective action to meet, or exceed, the application's real-time requirements.

As one thread waits to access the memory, other threads can be fed into the pipeline and executed which makes the system more efficient. The MIPS Technologies 34K cores can undergo minimal changes to run two-way symmetric

and 34Kf Pro which have CorExtend capability. This feature enables the addition of proprietary functions and tightly-coupled hardware. There is also the 34Kf, which adds hardware floating point support, compliant to the IEEE 754 specification.

All four cores can also be used where independent concurrent threads have different roles. This is known as asymmetric multiprocessing. They can also be configured with up to two virtual processing elements (VPEs) and five thread Contexts. The latter is a representation of the user-state of the MIPS32 architecture. This dual capability allows the cores to run two independent operating systems (OS) concurrently or can be used to run a two-way single-issue, multi-threaded pipeline OS.

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thread cores in its EyeQ2 SoC for cars' driver assistance and safety systems.

Using the cores in embedded system design, there is an increase in die size area. This increase is 14 per cent over a single-threaded processor, but this is compensated for with an increase in throughput. Internal benchmarks rated the 34Kc core, running two threads was 60 per cent faster than a single-threaded processor.

multiprocessing operating systems. Most embedded applications use asymmetric processing, yet it is the cores' symmetric configuration whereby the data is divided up for separate analysis, that makes the cores particularly suited to high-performance imaging applications. With the levels of power efficiency within the cores, they can be used in low-power applications, such as handheld, mobile devices, MP3 players and digital cameras.

Extended family

There are four members in the MIPS32 34K core family, all of which are available now. In addition to the 34Kc, there is the 34Kc Pro

Core support

The cores include OCP (on-chip protocol), the industry-standard IP core interface for plug-and-play SoC design as the native interface for all members of the family. There is also a scalable, intelligent interconnect architecture that boosts 34K-based system performance available from Sonics. The architecture is designed to make peripheral integration easier. The company's SMART Interconnects allows users to customise designs and reduce development time for SoCs.

EDA companies support the multi-thread cores, with Cadence making Encounter Reference Methodology available as well as its Incisive emulation co-verification and Palladium software debugger tools. Magma has also released a reference methodology based on Magma Blast Create RTL-to-placed gates, Blast Plan Pro hierarchical design and Blast Fusion for physical design solutions for the cores. Synopsys has optimised its Galaxy Design platform reference flow for the cores.

Other companies providing support to develop the cores are CoWare with its ConvergenceSC environment and Green Hills Software's software development solution. Similarly, Accelerated Technology supports the cores with its Nucleus RTOS and Eclipse-based Nucleus EDGE IDE. Express Logic's ThreadX RTOS is also available.

Microsoft has announced that its next version of Windows CE will run on the 34K core family and has made a board support package available from www.mips.com.

A software development environment supporting the cores is available free from the same website. A toolkit includes Free Software Foundation Open Source GNU tools with the company's proprietary runtime libraries that are pre-configured to popular evaluation boards. 