

Novas makes signals visible

It has become clear that there is a growing gap between first silicon and verification, writes CAROLINE HAYES. As a result, verification is suffering as there is a profusion of data that design engineers cannot see and so cannot predict the behaviour of a design.

Multiple iterations slow down the design time and add to the expense. Early in the design flow, signals can be 'dumped' but this is not practical in full-chip regression simulation and as the design moves into emulation and prototype stages, access to signal data is only through logic structures that have been inserted into the hardware.

Novas (www.novas.com) has introduced new levels of visibility to complex IC verification and system validation with the Siloti Visibility Enhancement suite. This takes initial signal information from the design to make all signals, including the unextractable parts, visible to the designer at the RTL (register transfer level) stage and completes the company's tool offerings from nESL, for high levels of abstraction, down to Verdi's RTL simulation debug suite.

The Siloti SiVE works with emulators, prototypes and DFD-enabled chips where it compiles the design and performs formal analysis to determine which signals are essential. Abstraction correlation and data expansion engines automatically map the chip's

low level structures up to the RTL and expand the dumped data to fill in the gaps.

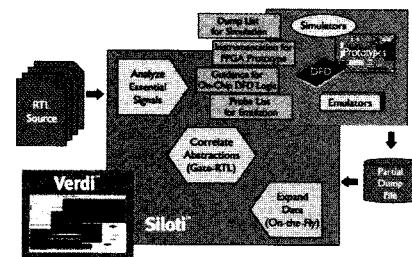
Siloti SimVE uses a methodology that limits dumping and eliminates multiple regression iterations. The company claims users can achieve a full-chip debug with a single regression run and minimal impact on the simulator performance.

There is an overhead associated with partial dumping, which Novas' Robert Ruiz, puts at 20 per cent.

Both tools are integrated with the company's Verdi automated debug system by extracting essential signals and expanding the data to fill in the missing parts to debug RTL using netlists. By analysing limited signal data and correlating complex low-level representations with RTL descriptions, debug cycles, with hardware emulation can be reduced by a factor of four, according to the company. Novas also claims that when used with DFD (design for debug) methodologies, visibility can be improved by a factor of five.

The two tools can be used with third-party simulation, emulation and FPGA-based prototyping tools, as well as DFD tools and test environments. The company has announced that ASIC and SoC prototyping system supplier, ProDesign, has integrated Siloti VE with its CHIPit Platinum V4 ASIC verification system (www.uchipit.com). The ASIC verification system is based on Xilinx's Virtex-4 FPGA and includes the HCD (host controller debugging)

tool which allows access to the FPGA's internal signal data to produce multi-million gate designs partitioned over multiple FPGAs quicker, by the ability to see internal signal activity, increasing the speed of verification and debug. Similarly, First Silicon Solutions (www.fs2.com) specialising in OCI (on-chip instrumentation) custom silicon IP, plans to support and be interoperable with Siloti SiVE. EDA company, DAFA (www.dafca.com) also supports SiVE in post-silicon debug and validation. The company focuses on SoC post-silicon debug and will integrate its reconfigurable instruments and diagnosis software with Siloti and Verdi tools. Novas has joined programmable logic supplier, Altera's ACCESS Program, designed to integrate and support complementary design technologies (www.altera.com). Initially, the two companies will develop interoperability between Altera's SignalTap II embedded logic analyser in its Quartus II development software and Siloti VE products.



Xilinx unveils next-Gen Virtex at 65nm

Xilinx (www.xilinx.com) continues its Virtex process roadmap, unveiling 65nm silicon in Monterey, California, last month. The die, produced by foundry partners Toshiba and UMC, continues the company's use of triple oxide II technology, used in the 90nm Virtex-4 introduced two years ago. The 65nm FPGAs will be available in the second half of this year, although the company has delivered software to beta customers through its early access programme.

Problems encountered as the process node reduces include balancing performance with voltage, maintaining low resistance levels and improving resolution for use for lithography.

The triple oxide technology, which uses three layers of oxides at different gate thicknesses, has been scaled to 65nm to reduce static power consumption, compared to traditional methods. With three layers, at three thicknesses, if the transistor does not need to be 'super-fast', then it can use the thicker oxide. Alternatively, fast, or fabric transistors

can use the thinner oxide.

Increasing the performance of transistors, relies on the mobility of electrons to move in the silicon. This mobility depends on crystal parameters, for example the lattice constant, which is the separation between silicon atoms. Intel pioneered the scaling process technique, introducing stress to the silicon close to the surface to change the lattice constant and modulate the mobility without increasing leakage, or parasitic currents. Mobility has to be increased to counter the current lost due to voltage reduction as the process geometry decreases. In essence, this translates to 1.2V at 90nm and 1V at 65nm. Reducing the voltage improves AC power and increased mobility boosts performance.

Transistor terminals have to be low resistance to avoid IR drops. They must also use the full voltage in the intrinsic transistor, so the source and drain have to be low resistance, as do the gate electrodes. While 90nm technologies use Cobalt Silicide, this

older material does not give the resistance low enough for the shortened gates. (At 65nm, the gate length is 40 to 50nm.) Xilinx uses nickel to lower the resistance and has found that it provides an extremely low junction leakage measured by the source/drain to substrate. Putting the source/drain and gate into silicon is done in a single step to make the silicon self-aligned, eliminating a lithography step.

At any process node, the resolution has to be proportional to the wavelength/numerical aperture (NA). In this development, Xilinx has used the same 193nm wavelength lithography, to capitalise on a proven technology, with the same scanners to achieve a higher NA than 90nm versions.

