Packaged solution?

Does SiP have a viable future as a poor man's SoC? By **Paul Dempsey**.

For some time, system in package (SiP) has been touted as the poor man's answer to system on chip (SoC). With eight figure NREs being presented as a potential norm for SoCs, such costs effectively rule out all but the biggest players.

By contrast, SiP's integration of separate silicon ics – many of which can be purchased off the shelf – is said to offer advantages in terms of cost and time to market. Yet SiP may still need a six figure investment.

At March's Globalpress Electronics Summit, a group of interested parties gathered to discuss the two approaches. Not surprisingly, the main conclusion was that there remains a great deal to resolve, both in terms of the SiP design process and its business models.

Perhaps the first telling reminder was that SiP was never intended as a rival to SoC in that 'discount integration' sense. "About 85% of SiPs are still used in cellphones and telecommunications," noted Gartner Dataquest analyst Jim Walker. "Part of the reason is that product life cycles are short. After six months, they would want to add an MP3 player. Six months later, they wanted to add a camera and so on.

Each iteration became more difficult an SoC, but SiP enabled those iterations. This, in turn, enabled SiPs to get into volume production and, from a manufacturing standpoint, the technology began to grow."

Scott Jewler, chief strategy officer for packaging research group STATS ChipPAC, seconded this view. "The application that has been the fastest to adopt SiP has been handsets. Over the last few years, there has been a transition from single chip package solutions into these multidie solutions and on to the ultimate solution of a handset in a package," he said.

"At the same time, handset functionality continues to increase, so I think the one or two package solution never happens – you have to add more silicon to get more functionality."

Obstacles to SiP

Mobashar Yazdani, manager of the asic program with Hewlett-Packard, highlighted some key obstacles as perceived by users. "There are some serious tools issues – and, in particular, design composition tools and concurrent design tools," he said.

"There is work happening on concurrent design, but not necessarily that much on composition. Yet we need tools that will allow us to look at the trade offs for different types of SiP. We need to

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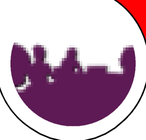

know which are really efficient and want to make the decisions ourselves."

Christine King, president of AMI Semiconductor, agreed that an ability to 'optimise the design point' is critical and that, often, the SoC against SiP choice was not as obvious as it might first appear.

"I want to give this example, because it is somewhat counter intuitive. We had one customer that was a washing machine company. For them, on a mid range solution, we used an 8051 microcontroller, embedded the flash right on the high voltage component and included high voltage relay drivers, led drivers and some precision sensors. In that case, we could do a limited number of complex calculations and didn't need a lot of flash. The ASP was $2.40 and it took about two years to get to full production on the component," she explained.

"When the same customer said it wanted a higher end system, we moved to a 16bit mcu, we needed a lot more flash – 2Mbit – and the integration here drove us to a more economical SiP solution with a $4.80 price and a faster development time. But it was the higher end application that drove us to SiP."

Jewler, meanwhile, believes there are two further aspects to the tools question. "The first is electrical design. There is some movement from the eda guys here on electrical management across multiple pieces of silicon. But there are mechanical challenges as well and these are significant cost drivers. Now, there are tools for this, but they work independently of the electrical tools," he said.

"So, you can optimise from an electrical standpoint and come up with an SiP solution that's more expensive than the SoC; whereas if you optimise from the mechanical standpoint, you may not achieve your performance target."

Yet more threats to SiP?

Outside the tools arena, Ivo Bolsens, CTO of Xilinx, believes there is another threat that may marginalise SiP's ability to make 'haves' out of SoC 'have nots'. And this is, in part, closely linked to where he sees an opportunity for fpgas within a package environment.

"Two things are needed to enable that [SiP] vision. The first is advanced SiP technology that can give you the bandwidth that you try to get today with SoCs – tens of thousands of interconnects between chips. The good news is that you can see start ups like Cubic Wafer and big companies like IBM and Infineon building that capability," he said.

"The second thing you need is a substrate on which you can build your system – and that's where I would like to position fpgas. I'd like to develop them as the virtual backplane; they have a rich programmable interconnect and you could build applications on that to build the capabilities of your system and leverage the bandwidth."

There is, however, a big catch. If no standard SiP interconnect can be developed, the technology will, in Bolsen's view, remain 'marginal'. And, beyond these technology requirements, there is one other elephant in the room.

"The really big issues are supplier issues," said HP's Yazdani. "With SiPs, you have a lot of suppliers to deal with. In SoC, you talk to one fab."

Other panelists sought to point out they could take on that system integrator type role. But he remained sceptical: "You may allow us to deal with one supplier, but the problem will remain that you have to talk to a lot of them – there is still an issue," he responded.

On the vendor side, Bolsens acknowledged a potentially serious issue. "The customer has to benefit from the business model and one problem I see here, with the accumulation of different silicon from different suppliers in an SiP, is an accumulation of their margins in that package."

For now, everyone expected SiP to grow rapidly in the near term, albeit from a position where SoC currently outsells it as a technology by a ratio of roughly 4:1. Whilst SiP does answer a number of immediate problems, there remain questions over its value as universal panacea.

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Jewler (right): "The application that has been the fastest to adopt SiP has been handsets."