

INTEGRATING IP AND WORKING IN UNITY

Intellectual property can differentiate silicon, defining features and capabilities within a design. CAROLINE HAYES looks at the options and integration issues

The need to patent ideas and enforce patents is a well-established notion. It helps to protect ideas and make them profitable, benefiting the creative source and rewarding investment in research and development. As technology and manufacturing moves to a global scale, with designers in one hemisphere and manufacturing facilities in another, companies have to look at the transfer of IP to be incorporated into products manufactured on another continent. Now, IP rights is more about protecting a block of IP while making sure it can be accessed and integrated without being illegally copied and reused.

Physical IP is memory, logic and I/O. To optimise yield, Virage Logic has embedded infrastructure IP into physical IP for to enhance test, diagnostics, repair and yield, as part of its Silicon Aware IP initiative. The initiative aims to increase yield at lower process geometries and to reduce time to volume production in the advanced process nodes. At present it is concentrating on 90nm and below process geometries.

Traditionally, independently optimised infrastructure IP and physical IP cannot work together. Add to this design complexities that increase as process nodes diminish, the incompatibility is just exacerbated. In addition, many IP specialists believe that such a 'bolt-on' approach adversely affects the SoC's area, speed and power qualities.

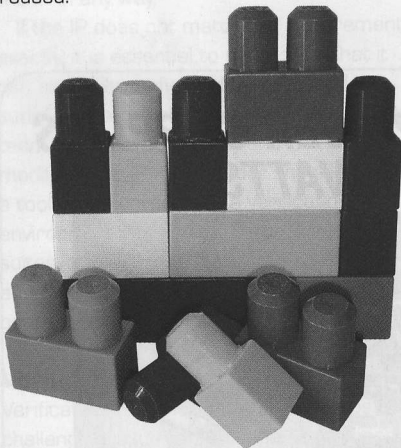
Infrastructure sharing

The company offers the STAR (Self-Test and Repair) Memory System which exploits the knowledge of physical IP in the infrastructure IP to improve yield and time to market while streamlining the process so that designers do not have to integrate or manage separate IP entities. It also means that the infrastructure can use specific knowledge of its traits to support the physical IP as well as the manufacturing process. The physical IP

can be created with an understanding of test, diagnostics, reliability and yield improvement algorithms, designed into the infrastructure. A single compiler generates the infrastructure and physical IP to save development time, as much of the structures are the same and can be shared.

Virage is also developing and licensing advanced embedded memory IP at the 65nm process node. Companies like Freescale Semiconductor licence the IPPrima Mobile Area, Speed and Power (ASAP) memory ultra-low power memories and its STAR memory system for mobile, baseband products where it can be used to address the power and performance management, high-volume manufacturing requirements for wireless consumer products at the lower geometry.

The ultra-low power memories can reduce static and dynamic power dissipation to extend a product's battery life. This is achieved by the memory having access to a range of power management methods to control static and dynamic power consumption. These include advanced optimisation techniques like block-level voltage islands, clock gating, mixed transistor



threshold voltage support, voltage and frequency scaling, back biasing and standby mode with state retention.

EDA IP

Companies are finding that they have customers in common and are collaborating to speed design and manufacture. For example, Taiwanese semiconductor foundry, UMC, uses Virage's IP and circuit design experience to develop its 65nm process technology. The partnership, announced last summer, is designed to accelerate adoption of the foundry's next-generation technology platform and provide a roadmap for IP structure enhancements, such as memory bit cells. At the lower process technologies, design and process teams have to liaise sooner in the design cycle than before to prevent some of the problems posed by the complexities of deep sub-micron technology nodes. As the attributes of 65nm technology, yield and performance improve, the technology will be adopted sooner and integrated into the mainstream of SoC design.

As part of this agreement, Virage Logic will collaborate with UMC's technology and design support teams to analyse process

parameters to design IP elements, memory, logic and I/O for example, to optimise the area, speed, performance and manufacturing yield of the resultant SoC.

Tool suites

Development tools are a part of the preparation for successful IP integration. For example, semiconductor design software supplier, Magma Design Automation, has created the MagmaTies programme, whereby IP vendors to create Magma-ready IP.

The programme encompasses vendors of ASICs, EDA tools, IP providers, service providers and semiconductor foundries. Vendors provide synthesis and reference methodology support for soft IP products and verification of industry-standard views for hard IP products, culminating in an IP portfolio for mutual customers to use. The IP can be integrated into complex IC designs to reduce time to market with an integrated solution.

There are 15 IP providers in the programme, with five new IP vendors recently joining; Aragio Solutions, Arteris, Go2silicon, SiWave and Soft Mixed Signal. Aragio Solutions specialises in custom digital

and analogue IC design. Its I/O libraries protect against ESD and provide high-latch immunity solution for ASIC designs. There are industry-standard interfaces, RF and analogue circuitry in the library.

Arteris provides a configurable network on chip (NoC) sub-system for SoC communications designs within the programme. Go2silicon has optimised and integrated its high-performance, analogue and mixed-signal IP cores with Magma's tools.

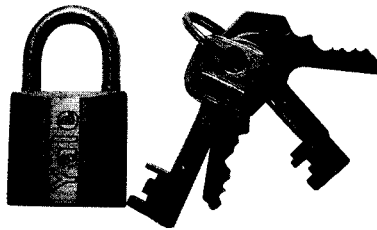
Two companies offer PHY IP in the programme. SiWave provides its PHY IP range for configurable and scalable 802.16/WiMax products that can be implemented for power-efficient IP for next-generation portable and mobile WiMax applications. Soft Mixed Signal Corporation offers its system-level PHY and transceiver IC solutions for LAN, WAN and SAN connectivity. The programme provides customers with the option to use proprietary mixed-signal and DSP technologies while developing a methodology for certifying IP block performance using Magma's Blast Wrap tool.

Uniform SoC IP

As demonstrated by this snapshot of different uses, development and delivery methods of IP, there is a case for commonality across the IP developer and user. Denali Software has initiated an industry alliance to promote industry-wide adoption of a Register Description Language (RDL) to develop and deliver IP used in SoC designs.

The RDL Alliance is intended to give a common, consistent and computer-readable format for describing configuration registers to speed up a chip's architecture, design, verification and documentation. There are configuration registers, often thousands, in all semiconductor chips and IP products. System architects, hardware developers and software engineers use the registers, which store key parameters to define a chip's operation. Alliance members can access Denali's Blueprint software to take RDL input and automatically generate documentation, register designs in Verilog or VHDL, and generate models for verification and software development. Blueprint also provides an abstraction layer that insulates customers from design or architectural changes during IP modifications or derivative

designs. This layer creates a stable environment for early hardware and software development. To further increase productivity and improve development methodology, the software also enables IP vendors to auto-generate outputs that



support methodologies and third party development tools used by customers. Denali's chief technology officer, Mark Gogolewski is chair of the Alliance. He describes the thinking behind the Alliance formation as 'We've created a practical program that offers immediate gains in productivity to IP providers and consumers, without requiring a methodology overhaul.' He goes on to explain 'It is critical to address chip design productivity, from architecture and design through verification and software development. This is particularly true for IP-based methodologies'. Charter members are

Mentor Graphics, MIPS Technologies and Rambus, all of whom will use RDL for the design and delivery of select IP products.

Estimating IP

ASIC and SoC designers can access and download IP developed by Giga Scale IC's IP Partner Program members at ChipEstimate.com. The website contains IP, foundry and economic data across the supply chain which is aggregated for estimates by semiconductor design houses, ASIC vendors and design service companies. The EDA company supplies InCyte, an estimation and analysis tool to the website which is used to estimate and quantify effects of IP in terms of parameters such as size, power, leakage yield and cost. Canadian Semiconductor Elliptic, a security IP provider, is the latest company to join the IP Partner Program offering semiconductor and embedded software. Its specialised IP includes AES (advanced encryption standard) and DES (data encryption standard) core algorithms, supported through single-purpose or dual-capability and ECC (Elliptic Curve Cryptography) cores as well as true and pseudo-random number generator functions.